

FORM PTO-1449

U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.  
MIC-40APPLICATION NO.  
10/722,959APPLICANT  
Seong-Hoon LeeCONFIRMATION NO.  
Not Yet AssignedFILING DATE  
November 26, 2003GROUP 2816  
~~Not Yet Assigned~~INFORMATION DISCLOSURE STATEMENT  
BY APPLICANT

## U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
<i>AK</i>	5,463,337	10/31/95	Leonowich	327	158	
<i>AK</i>	6,194,947 B1	02/27/01	Lee et al.	327	359	
<i>AK</i>	6,295,328 B1	09/25/01	Kim et al.	375	376	
<i>AK</i>	6,313,688 B1	11/06/01	Lee et al.	327	359	
<i>AK</i>	6,326,826 B1	12/04/01	Lee et al.	327	161	
<i>AK</i>	6,366,148 B1	04/02/02	Kim	327	262	
<i>AK</i>	6,512,408 B2	01/28/03	Lee et al.	327	359	
<i>AK</i>	6,573,771 B2	06/03/03	Lee et al.	327	158	
<i>AK</i>	6,642,760 B1	11/04/03	Alon et al.	327	158	
<i>AK</i>	6,661,863 B1	12/09/03	Toosky	375	376	
<i>AK</i>	2003/0219088 A1	12/30/02	Kwak	375	376	

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER INITIAL	
<i>AK</i>	Jong-Tae Kwak, <u>A Low Cost High Performance Register-Controlled Digital DLL for 1 Gbps x32 DDR SDRAM</u> , The 8th Korean Conference on Semiconductors, February 2001.
<i>AK</i>	Ramin Farjad-Rad, <u>A Low-Power Multiplying DLL for Low-Jitter Multigigahertz Clock Generation in Highly Integrated Digital Chips</u> , IEEE Journal of Solid-State Circuits, Vol. 37, No. 12, December 2002, p. 1804-1812.

All references have been considered.

*AK*  
EXAMINER INITIAL

EXAMINER

*LLM*

DATE CONSIDERED

*11/23/04*

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not conformance and not considered. Include copy of this form with next communication to applicant.